IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

REMARKS

Rejections Under 35 U.S.C. §112, Second Paragraph.

Claim 1 has been amended to address this ground of rejection.

Rejection of Claims 1-23 Under 35 U.S.C. §103(a), based on *Baxter* (U.S. Patent No. 5,815,405) in view of *Jefferson* (U.S. Patent 6,127,865).

The rejection of claims 1-14 will first be addressed.

The invention of amended claim 1 is directed to an integrated circuit device that includes a programmable portion with a plurality of circuits that may be configured by a user of the integrated circuit device. The integrated circuit device also includes at least one communication portion. The communication portion includes at least one circuit block manufactured to perform a predetermined data communication function including converting received first data values into second data values.

As is well understood, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

A prima facie case of obviousness has not been established for claim 1, as the cited references do not show or suggest all claim limitations and there is no motivation for combining the references as set forth in the rejection.

The cited combination does not show or suggest an integrated circuit having both a programmable portion and a communication portion, where the communication portion converts first data values into second data values, as recited in claim 1.

Baxter does not show such a limitation. *Baxter* shows a programmable logic device (PLD) having configurable elements and (optionally) "transparent circuits." Such transparent circuits are never shown or suggested to provide any kind of data value conversion.[1]

[1] See *Baxter*, FIG. 1A, and Col. 3, Lines 28-51, which describes transparent circuit examples of: an oscillator clock divider or a boundary scan circuits. These circuits do not convert data values.

The second reference relied upon, *Jefferson*, teaches a PLD having a phase lock loop circuit for providing a time shifted clock network for the PLD. Such a circuit does not provide a data value conversion, thus is not believed to be suggestive of the claim 1 limitations.

The last reference relied upon, Applicants' *Background Art*, does not show such a limitation, and has been misquoted in supporting the rejection. Applicants' claim 1 recites a circuit block manufactured to perform a predetermined data communication function. In very sharp contrast, the submitted *Background Art* describes programming a PLD to provide a communication function – essentially the exact opposite to what is claimed.[2] That is, the *Background Art* teaches programming circuits to provide a data communication function and not providing circuit blocks manufactured to provide such functions. Thus, the *Background Art* teaches away from the claim limitations.

Thus, because the references do not show all limitations of claim 1, a prima facie case of obviousness has not been established for claim 1.

In addition or alternatively, the references relied upon teach away from the invention, and teach away from the combination. Thus, there is no suggestion or motivation for the combination relied upon by the rejection.

The reference *Baxter* teaches away from the invention of claim 1. Applicants believe a clarification of the teachings set forth in *Baxter* is in order. *Baxter* is directed to non-programmable integrated circuits. In particular, *Baxter* teaches a method for using circuit design information for a PLD to manufacture a non-programmable integrated circuit having the same function. The rejection states

> [*Baxter*] teaches a programming circuit that communicates with another part of the logic device via buses and the generation of a bit stream (see Figure 1B).

This is not correct. Figure 1B of *Baxter* illustrates a method carried out on a computer and provides no teachings regarding programming circuits or data buses. This is explicitly stated in the reference:

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[2] See Applicants' Specification, Page 2, Line 15 to Page 4, Line 9. In this portion, Applicants' describe encoding/decoding schemes, but clearly indicate that such functions are conventionally implemented by programming a PLD, not by manufacturing a circuit block to perform such a function.

This embodiment is implemented using one or more computers.[3]

If reference is made to Figure 1B of *Baxter*, it is clear that the end result of the process is a "new integrated circuit" 190, which has been fabricated to be non-programmable.[4]

In contrast to the teachings of *Baxter*, Applicants' claim 1 invention is directed to an integrated circuit that includes both a programmable portion and a communication portion. As shown above, *Baxter* teaches the formation of non-programmable integrated circuits using configuration data for programmable integrated circuits. Accordingly, the teachings of *Baxter* weigh against combining both programmable and non-programmable portions on the same integrated circuit – as set forth in claim 1.

Numerous dependent claims have limitations either not shown by the reference, or not addressed in the rejection.

Claim 3 recites a memory circuit that stores configuration information for configuring circuits of the programmable portion. This limitation was not addressed by the rejection. No citation has been provided showing which reference shows or suggests a memory circuit with the above claimed function (storing configuration data). Accordingly, a prima facie case of obviousness cannot have been established for claim 3.

Claim 5 recites a plurality of input/output (I/O) circuits commonly connected to both the programmable portion and the communication portion. No citation has been provided showing which reference shows or suggests such an I/O circuit connection. Accordingly, a prima facie case cannot have been established for claim 5.

Claim 6 recites a communication portion having the very particular limitation of multiple data operation circuits that each perform a different function on received input data. No citation has been provided showing which reference shows or suggests such a limitation. Accordingly, a prima facie case of obviousness cannot have been established for claim 6.

Claims 9-11 recites variations on a communication portion with an operational control store. The operational control store provides operational values to data operation circuits that control the particular type of operation preformed on input data. No citation has been provided

[3] See *Baxter*, Col. 3, Lines 64-65.

showing which reference shows or suggests such a limitation. Accordingly, a prima facie case of obviousness cannot have been established for claim 9-11.

Claim 12 recites a data multiplexer (MUX) with a particular function. No mention is made of such a limitation in the rejection. Accordingly, no prima facie case of obviousness can exist for this claim.

Claim 13 recites a communication portion that includes a physical layer circuit. No mention is made of such a limitation in the rejection. Accordingly, no prima facie case of obviousness can exist for this claim, either.

In summary, Applicants' do not believe a prima facie case of obviousness has been established for claim 1, and cannot have been established for claims 3, 5, 6, 9-13. Thus, the rejection of claims 1-14 is traversed.

The rejection of claims 15-20 will now be addressed.

The invention of claim 15 is directed to a programmable logic device having a communication portion embedded therein. The communication portion includes non-programmable circuits designed to provide a selectable data communication function.

A prima facie case of obviousness cannot have been established for this claim. The limitation of "non-programmable circuits designed to provide a selectable data communication function" is simply not addressed in the rejection. If the examiner believes that this limitation is shown, Applicants respectfully request a citation.

Thus, because no reasons for rejection have been provided for claim 15, this rejection is improper, and should be withdrawn.

For this reason alone, the rejection of claims 15-20 is traversed.

The rejection of claims 21-23 will now be addressed.

The invention of amended claim 21 is directed to method that includes performing predetermined logic functions on a programmable logic portion of the integrated circuit. The method also includes performing serial data communication functions on a communication

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[4] See *Baxter*, Col. 7, Lines 4-9, which describes how the new integrated circuit has the functions of the PLD, but is not PLD, but rather an integrated circuit manufacture by a foundry.

portion of the integrated circuit that includes circuit blocks that are not formed with programmable logic device configuration data.

A prima facie case of obviousness has not been established for claim 21, as all limitations of the claim are not shown or suggested by the cited references.

As noted above, *Baxter* shows a programmable logic device (PLD) that may optionally include "transparent circuits." However, such transparent circuits are never shown or suggested to perform serial data communication functions.[5] Further, because *Baxter* is aimed at forming a new (non-PLD) integrated circuit from PLD configuration data, such a reference is believed to teach away from the claimed method, which executes different functions on a programmable logic portion and circuit blocks that are not formed with PLD configuration data. The reference *Baxter* would create an entire integrated circuit from PLD configuration data.

The second reference relied upon, *Jefferson*, teaches a PLD having a phase lock loop circuit for providing a time shifted clock network for the PLD. Such a circuit does not provide a serial data communication functions, thus is not believed to be suggestive of the claim 21 limitations.

The last reference relied upon, the *Background Art*, does not show all limitations of claim 21. As noted above, the *Background Art* teaches that serial data communication functions that are formed (e.g., synthesized) by programming programmable logic circuits according to configuration data. This is the opposite of what is set forth in claim 21. Thus, the *Background Art* teaches away from claim 21.

Thus, because the combination of references relied upon by the rejection does not show all limitations of claim 21, and the reference are believed to teach away from the method of claim 21, a prima facie case of obviousness has not been established. Accordingly, the rejection of claims 21-23 is traversed.

[5] See *Baxter*, FIG. 1A, and Col. 3, Lines 28-51, which describes transparent circuit examples of an oscillator clock divider or a boundary scan circuits.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Claims 1 and 21 have been amended to more clearly describe the invention, and not in response to the cited art. The present claims 1-23 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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Bradley T. Sako
Attorney
Reg. No. 37,923

Bradley T. Sako
WALKER & SAKO, LLP
300 South First Street
Suite 235
San Jose, CA 95113
Tel. 1-408-289-5315

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Version With Markings to Show Changes Made

In the Claims.

1. (Amended) An integrated circuit device, comprising:

a programmable portion comprising a plurality of circuits **[that may be]** configur**able[ed]** by a user of the integrated circuit device; and

at least one communication portion comprising at least one circuit block manufactured to perform a predetermined data communication function including converting received first data values into second data values.

21. (Amended) A method, comprising the steps of:

performing predetermined logic functions on a programmable logic portion of the integrated circuit; and

performing serial data communication functions on a communication portion of the integrated circuit that includes circuit blocks that are not **formed [synthesized] with programmable logic device configuration data**.